Docket No.: U2054.0107

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Junji Tajime et al.

Application No.: 09/334,354 — Confirmation No.: 5240

Filed: June 16, 1999 — Art Unit: 2613

For: MOVING PICTURE DECODING APPARATUS AND MOVING PICTURE DECODING METHOD — Examiner: R. J. Lee

APPEAL BRIEF

U.S. Patent and Trademark Office
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Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on July 29, 2005, and is in furtherance of said Notice of Appeal.

You are hereby authorized to charge our credit card for the fee of $500.00 required under Section 1.17(f). PTO Form 2038 is attached.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2215.

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CONTINGENT EXTENSION REQUEST

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 CFR 1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 CFR 1.135. The fee under 37 CFR 1.17 should be charged to our Deposit Account No. 50-2215.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

NEC Corp.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 18 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 1-18
4. Claims allowed: None
5. Claims rejected: 1-18

C. Claims On Appeal

The claims on appeal are claims 1-18

IV. STATUS OF AMENDMENTS

Appellant filed an Amendment After Final Rejection on June 15, 2005. The Examiner responded to the Amendment After Final Rejection in Advisory Actions mailed June 24, 2005 and July 8, 2005. In the Advisory Action, the Examiner indicated that

Appellants' proposed amendments to claims 1-2, 9-10, 12, and 17 would be entered, thereby overcoming the Examiner's rejection under 35 U.S.C. § 112, first paragraph.

Accordingly, the claims enclosed herein as Appendix A incorporate the amendments to claims, as indicated in the paper filed by Appellant on June 15, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a moving picture decoding apparatus. See Specification, pg. 1, lns. 4-6. In particular, the picture decoding apparatus uses memory access unit width, i.e., the bus width of the bus accessing the memory unit, in a memory compression and expansion section for bit allocation during quantization. See Specification, pg. 2, lns. 5-10.

In the moving picture decoding apparatus, compression is applied to a decoded image in a memory compressor 105. The compressed decoded image is stored in a frame memory 106. Based on the contents in the frame memory 106, a memory access width control section 110 applies control to a quantizer control section 109 so that the number of coded data bits is conformed to be equal to or less than the number of bits of the memory access unit. In other words, the coded data bits are equal to or less than the bus width of the bus that accesses the memory.

As shown in Figure 1, a compressed moving pictures stream encoded by a system, such as an MPEG-2 video system, is supplied as an input to variable length decoder 101. The variable length decoder 101 performs variable length decoding and supplies a result to the inverse quantizer 102. The inverse quantizer 102 performs inverse quantization and supplies the result to an inverse discreet cosine transducer 103, which transduces a conversion coefficient into an image and supplies the result to adder 104. Adder 104 performs addition of the image supply from the inverse discreet

cosine transducer 103 and a predicted image supplied from the motion compensation section 108 and supplies a result to the memory compression and expansion section 11. The memory compression and expansion section performs compression and expansion operations to a decoded image and supplies it to the motion compensation section 108. See specification, pg. 7, lns. 5-21.

Memory compressor 105 of the memory compression and expansion section 11 applies compression to the image supplied from adder 104 and stores the compressed results in frame memory 106. Memory expander 107 extracts the compressed image from the frame memory 106 and expands it, supplying the expanded result to the motion compensation section 108. The quantization control section 109 applies control of quantization of the image to the memory compressor 105 and the memory expander 107. The access width control section 110 applies control to the quantization section 109 using information of the frame memory 106 so that the information content for a single or a plurality of memory compression processing units or for every control unit of the memory compression process is conformed to be equal to or less than the number of bits of a memory access unit (the bus that accesses the memory unit). See specification, pg. 8, lns. 1-17.

Figure 4 illustrates an arrangement of the memory compression and expansion section according to the present invention. As shown in Figure 4, an image to be compressed is supplied to subtractor 201 as an input which performs subtraction of this input signal and a predicted value supplied from predictor 206 and supplies a prediction error to the quantizer 202. Quantizer 202 performs quantization of the prediction error in accordance with the quantization control section 24 and supplies the result to the fixed length encoder 203 and the inverse quantizer 204. The fixed length encoder 203 encodes the quantized value and stores it in the frame memory 22.

Inverse quantization and local decoding are performed in inverse quantizer 204, adder 205 and predictor 206 and an output of predictor 206 is supplied to subtractor 201.

The memory access width control section 25 takes into account a compression ratio based of an occupied ratio of the frame memory 22, and applies bit allocation control to the quantization control section 24 which conforms to the number of bits of a memory access unit. See specification, pg. 9, lns. 13-16. The quantization control section 24 performs quantization control in which memory access width information is added and applies control to the quantizer 202 so that information content generating for a single or plurality of memory compression processing units or for every control unit of the memory compression processes equal to or less than the number of bits of a memory access unit. See Id. lns. 17-21.

In another example, one quantizer having a fixed compression ratio is used for quantization of a prediction error. When that information content generated exceeds the number of bits of a memory access unit, a plurality of quantizers are prepared and controls conducted so that the information content conforms with the access width. See Specification, pg. 10, lns. 1-8. This arrangement can be adopted in an arrangement where a plurality of quanitzers having quantization characteristics different from each other share one quantization characteristic table. Thus, as discussed above, the quantization is conducted with respect to the memory access unit (the width of the bus accessing the memory, as opposed to the size of the memory itself).

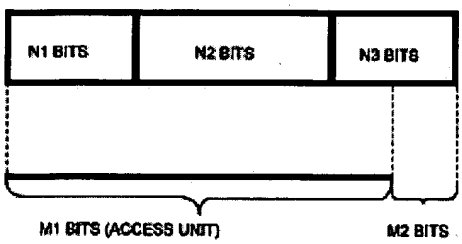

FIG.2

As shown in Figure 2 reproduced above, the memory access unit is M1 bits. The coded data bits of the compression processing units are N1, N2, and N3. As shown, the coded data cannot be extracted through one access because the width of the access unit is less than the N1, N2, and N3 bits. Thus, the bit allocation should be reduced to be equal to the M1 bits of the access unit.

In contrast, as shown in Figure 3 reproduced below, the number of allocated bits is less than the number of bits M1 of the memory access unit. As shown in Figure 3, the allocation of the number of bits of the coded data can be increased so that it is equal to the M1 bits of the access unit.

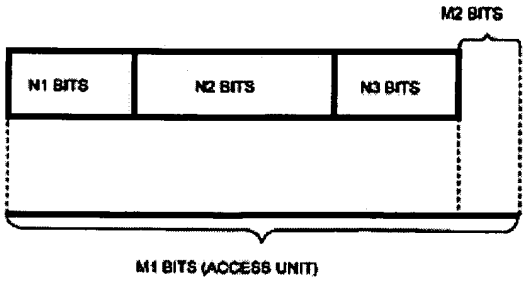

FIG.3

According to the present invention, the memory access width control section 110 controls the quantization control section so that the number of coded data bits is equal to or less than the number of bits of the memory access unit (the bus width of the

bus that accesses the memory access unit). Based on the access width information from the access width control section, quantization control is conducted by preparing a plurality of quantizers having different quantization characteristics and a quantization table by selecting a quantizer that is adapted to the access width. See Specification at 6, lns. 4-15.

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

The rejection of claims 1-14 and 16-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,208,689 ("Ohira").

The rejection of claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Ohira in view of U.S. Patent No. 6,243,421 ("Nakajima").

VII. ARGUMENT

Claims 1-18 are pending in this application. Claims 1-18 stand rejected under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a). Appellant respectfully submits that each of the pending claims is in immediate condition for allowance and requests withdrawal of the pending rejections.

A. The invention defined in claims 1-18 is patentable over U.S. Patent No. 6,208,689 ("Ohira").

Paragraph 4 of the Final Office Action rejects claims 1-14 and 16-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,208,689 ("Ohira"). Appellants respectfully request reconsideration and withdrawal of this rejection.

To anticipate a claim under 35 U.S.C. § 102, the cited reference must disclose every element of the claim, as arranged in the claim, and in sufficient detail to enable one skilled in the art to make and use the anticipated subject matter. See, PPG

Industries, Inc. v. Guardian Industries Corp., 75 F.3d 1558, 1566 (Fed. Cir. 1996); C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1349 (Fed. Cir. 1998). A reference that does not expressly disclose all of the elements of a claimed invention cannot anticipate unless all of the undisclosed elements are inherently present in the reference. See, Continental Can Co. USA v. Monsanto Co., 942 F.2d 1264, 1268 (Fed. Cir. 1991).

Among the limitations of Appellants' claims not shown or disclosed in Ohira is a memory access width controller that controls said quantization controller such that bit allocation is controlled in relation to a number of bits of the memory bus that accesses said memory. Ohira is silent as to this limitation.

The Examiner merely repeats the rejection set forth in the Office Action of September 24, 2003 and the further description of the rejection in the Final Office Action dated March 5, 2004, in which the Examiner asserted that Ohira teaches that the compression rate judging section 106 judges a rate of the decoded data 151 and stored in the frame memory based on the size of the image in connection with the storage capacity of the frame memory. The compression rate judging section 106 selects a compression mode from among the plurality of compression modes based on the rate of compression. Ohira states that the compression rate is decided based on the storage capacity and the image size.[1] The storage capacity is discussed at column 13, line 20 *et seq*. Specifically, Ohira states

> The predictive/display frame memory section 103 including frame memory, being assigned a predetermined storage capacity stores image data on a frame basis. The

[1] The compression judging rate section providing the rate of compression in connection with the storage capacity of the frame memory 103 utilizes the expression T x U x R/LM £ Z with Z being the number of bits within memory 103 and LM being the rate of compression. Z represents the size of the memory, not the width of the data bus accessing the memory.

> compression rate judging section 106 receives the image size information 156 including the size of image of the encoded data 150. The compression rate judging section 106 judges a rate of the decoded data 151 to be compressed and stored in the frame memory based upon the size of the image in connection with the storage capacity of the frame memory.

This merely means that the image data is stored in a predetermined storage capacity on a frame basis. However, at no time does Ohira discuss the bus accessing the memory (the memory access unit).

Appellants specifically disagree that the storage capacity referred by Ohira reads on the number of bits of the memory access unit as claimed. Ohira's storage capacity is described at column 13, line 20 *et seq.* refers to the capacity of the frame memory, not the width of the bus that accesses the memory. For example, there are various memories having the same capacity of 128 megabytes of which the data bus width (equivalent to the number of bits of a memory access unit) is 8 bits, 16 bits, 32 bits, etc. In a case where the teaching of Ohira is used, the compression data rate is not altered because the frame memory capacity is the same 128 megabytes, even though a different data bus width is employed. On the other hand, where the claimed invention is used, when the memory having a different data bus is employed, the data compression rate is altered.

In other words, according to Appellants' explicitly recited claim, in the present invention, not only the storage capacity and the size of the image affect the compression rate but also the number of bits of a memory access unit specific to the memory. In contrast, in the Ohira reference, the width of the access bus is never taken into account. As such, the Ohira reference fails to disclose Appellants' explicitly recited claims.

The Examiner equates Ohira's storage memory with the memory access unit of the present application. The Examiner asserts "the memory access unit is equivalent to a storage capacity of the frame memory." See Interview Summary, May 13, 2005. This is incorrect. The memory access unit provides access to a memory. See specification pg. 5, lns. 27, et seq. In contrast, the storage memory stores data input via the memory access unit. Thus, the storage memory is different than the memory access unit.

The number of bits of the memory access unit is different than the number of bits of the storage unit itself. In other words, the claimed memory access unit is equivalent to an entrance ramp of a parking garage and the storage memory disclosed in Ohira is equivalent to the parking garage accessed by the entrance ramp. It would be improper to equate the number of parking spaces in a parking garage with the size of the entrance ramp. Likewise, it is improper to equate the size of Ohira's storage memory with the size of Appellants' memory access unit. Further, Ohira neither discloses nor suggests varying bit allocation, i.e., the number of coded bits, as a function of the size of the memory access unit. In fact, Ohira is completely silent as to the memory access unit.

The Examiner asserted that the Z number of bits within the memory is equivalent to the bus accessing the memory. However, this is incorrect, as the bus accessing the memory can be any number of bits wide regardless of the size of the actual memory. Appellants respectfully submit that Ohira fails to consider the number of bits of the memory bus that accesses the memory in performing a decoding operation. Thus, Ohira fails to disclose Appellants' invention.

Because Ohira fails to disclose or suggest controlling bit allocation as a function of the number of bits of the memory access unit, Appellants respectfully submit

that the rejection under 35 U.S.C. § 102(e) should be withdrawn and the claims passed to issue.

B. The invention defined in claim 15 is patentable over Ohira in view of U.S. Patent No. 6,243,421 ("Nakajima").

As discussed above, Ohira fails to disclose controlling bit allocation in relation to a number of bits of the memory access unit of said memory. Nakajima was not included to cure this deficiency but to disclose an additional limitation which, even if it were to show, does not cure the deficiency in Ohira discussed above. Therefore, Appellants respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a).

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Appellant on June 15, 2005, and do not include the amendment(s) filed on June 15, 2005.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: September 28, 2005

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/334,354

1. A moving picture decoding apparatus to which a compressed stream generated using inter-frame prediction is input, said apparatus comprising:

a compressor that compresses a decoded image and stores the resulting compressed image in a memory;

an expander that expands a compressed image stored in said memory;

a quantization controller that controls how quantization is performed in said compressor; and

a memory access width controller that controls said quantization controller such that bit allocation is controlled in relation to a number of bits of a memory access unit of said memory.

2. The moving picture decoding apparatus according to claim 1, wherein said memory access width controller controls said quantization controller such that a number of coded bits of the image processed in said compressor for every control unit of compression processing is in conformity with the number of bits of the memory access unit of said memory in the case that the coded number of bits exceeds the number of bits of the memory access unit of said memory.

3. The moving picture decoding apparatus according to claim 1, wherein the compressor and the expander conduct compression and expansion, respectively, in accordance with a pixel difference prediction encoding system.

4. The moving picture decoding apparatus according to claim 1, wherein said quantization controller controls quantization by preparing a plurality of quantizers and a plurality of quantization characteristic tables.

5. The moving picture decoding apparatus according to claim 1, wherein said quantization controller controls quantization by preparing a plurality of quantizers and a quantization characteristic table being shared by said plurality of quantizers.

6. The moving picture decoding apparatus according to claim 1, wherein the compressor and the expander conduct compression and expansion, respectively, in accordance with an orthogonal translation encoding system.

7. The moving picture decoding apparatus according to claim 1, wherein said memory access width controller conducts control using information included in the compressed stream.

8. The moving picture decoding apparatus according to claim 1, wherein the memory is a frame memory.

9. A moving picture decoding apparatus to which a compressed stream generated using inter-frame prediction is input, said apparatus comprising:

a compressor that compresses a decoded image;

a memory that stores the compressed image output from said compression means compressor;

an expander that expands the compressed image stored in said memory;

a quantization controller that controls how quantization is performed in said compressor; and

a memory access width controller that applies bit allocation control to said quantization controller based on the number of bits of a memory access unit of said memory,

wherein said quantization controller controls quantization performed by the compressor based on access width information from said memory access width controller such that a number of bits of the image processed in said compressor for every control unit of compression processing is equal to or less than the number of bits

of the memory access unit of said memory in the case that the number of bits for every control unit of compression processing exceeds the number of bits of memory access unit of said memory.

10. The moving picture decoding apparatus according to claim 9, wherein said memory access width controller applies bit allocation control to said quantization controller in conformity with the number of bits of the memory access unit of said memory, based on an occupied content of said memory.

11. The moving picture decoding apparatus according to claim 9, wherein the memory access width controller conducts control using information included in the compressed stream.

12. The moving picture decoding apparatus according to claim 9, wherein the memory access width controller applies control to the quantization controller such that when an allocated number of bits of coded data of a compression processing block exceeds the number of bits of the memory access unit of said memory or is less than the number of bits of the memory access unit of said memory, the allocated number of bits is made equal to or less than the number of bits of the memory access unit of said memory by subtracting a predetermined number of bits from the allocated bits of coded data of said compression processing block or by increasing the number of allocated bits by the predetermined number of bits, whereby the coded data is enabled to be extracted from said storage means memory with one access occurrence.

13. The moving picture decoding apparatus according to claim 9, wherein the compressor controls quantization characteristics used for quantizing said decoded image, based on control by said quantization controller.

14. The moving picture decoding apparatus according to claim 9, wherein said quantization controller controls quantization by preparing a plurality of quantizers having

quantization characteristics different from each other, and wherein a quantization characteristic table is shared by said plurality of quantizers.

15. The moving picture decoding apparatus according to claim 9, wherein said compressor comprises a subtracter, a quantizer, an encoder, an inverse quantizer, an adder and a predictor, a prediction error obtained in said subtracter by a subtraction operation between said decoded image and a predicted value from said predictor is supplied to said quantizer, under control of said quantization controller, said quantizer quantizes said prediction error and supplies the quantized result to said encoder and said inverse quantizer, said encoder encodes an output from said quantizer and outputs the encoded result to said storage means memory, and inverse quantization and local decoding are conducted in said inverse quantization, said adder, and said predictor.

16. The moving picture decoding apparatus according to claim 9, wherein the memory is a frame memory.

17. A moving picture decoding method comprising the steps of:

detecting a number of coded bits for every control unit of compression processing and controlling said number of coded bits so that said number of coded bits is in conformity with the number of bits of a memory access unit of a memory when said detected number of coded bits exceeds the number of bits of a memory access unit of said memory.

18. The moving picture decoding method according to claim 17, wherein said step of controlling comprises using information from an external compressed data stream.